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Implementation of an Efficient Pulse-Triggered Flip Flop for Ultra Applications

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Abstract: **A huge portion of the on chip power is stimulated by the clock system which is made of the clock distribution network and flop-flops. In synchronous systems, high speed has been achieved using sophisticated pipelining techniques.**

In this scrutiny we introduce a new Dual dynamic node hybrid flip-flop and a novel embedded logic module based on DDFF. These flip-flops are based on the D flip-flop and latch embedded logic. This logic uses basic gates and universal gates and also Comparing the performance of DDFF with other Flip-flops which are designed for low power and high performance. The basic features of these flip-flops are highlighting and appraise them based on power consumption, speed. The foremost aim is an AND function is removed from the critical path to facilitate a faster discharge operation. Instead of this we are using a simple two transistor AND gate design is used for the reduction of complexity.

To introduce the conditional pulse enhancement for speed up the discharge swing along the critical path only when needed. For saving the power we can reduce the transistor sizes which are used at delay inverter and pulse generation circuit.

Keywords: **Embedded logic, flip-flops, high-speed, leakage power, low-power.**

I. INTRODUCTION

Flip-Flops FFs) are the basic storage elements used extensively in all kinds of digital designs. In particular, digital designs nowadays often adopt intensive pipelining techniques and employ many FF-rich modules. It is also estimated that the power consumption of clock system, which consists of clock distribution networks and storage elements, is as high as 20%-45% of the total system power. In recent VLSI's, a clocking system, including clock interconnections and flip flops. This is partially because the activation ratio of a clock system is unity. In this clocking system power, 90% is consumed by the last branches of the clock distribution network which derive directly F/F's and the F/F's them selves. P-FF has been considered a popular alternative to the conventional master slave based FF in the application of high speed operations. High performance flip flops are key elements in the design of contemporary high-speed integrated circuits. In these circuits, high clock frequencies are generally gained by using a fine grain pipeline in which only few logic levels are inserted between pipeline stages. In this paper, we will present a novel low-power implicit-type P-FF design featuring a conditional pulse-enhancement scheme. Three additional transistors are employed to support this feature. In spite of a slight increase in total transistor count, transistors of the pulse generation logic benefit from significant size reductions and the overall layout area is even slightly reduced.

1. Conventional Implicit-Type P-FF Designs:

ip-DCO

Some conventional implicit-type P-FF designs, which are used as the reference designs in later performance comparisons, are first reviewed. A state-of-the-art P-FF design, named ip-DCO, is given in Fig 1(a) . It contains an AND logic-based

pulse generator and a semi-dynamic structured latch design. Inverters I5 and I6 are used to latch data and inverters I7 and I8 are used to hold the internal node. The pulse generator takes complementary and delay skewed clock signals to generate a transparent window equal in size to the delay by inverters I1-I3. Two practical problems exist in this design. First, during the rising edge, n MOS transistors N2 and N3 are turned on.

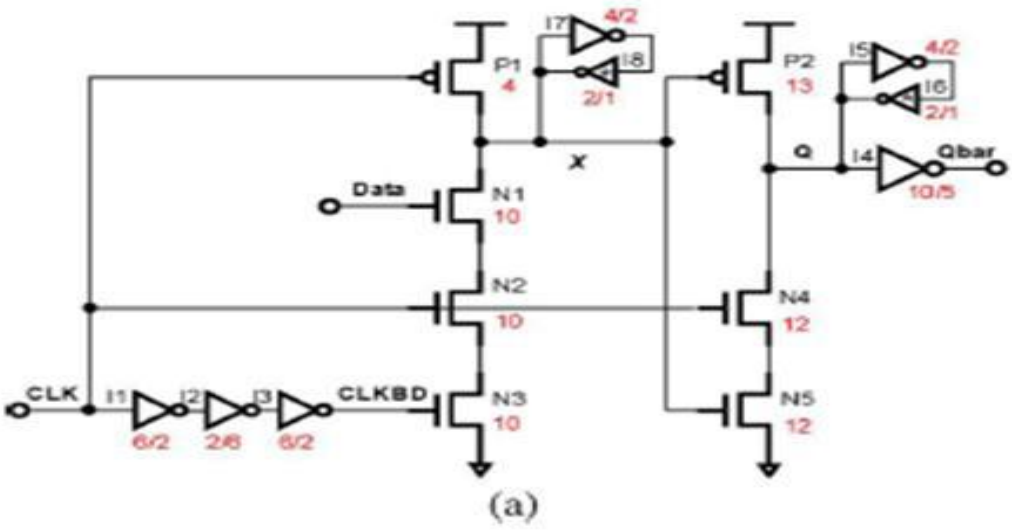

Fig. 1(a) ip-DCO

Both equal to "1". Extra DC power emerges if node X is drifted from an intact "1".

2. Implicit-Type P-FF Design with Pulse Control Scheme

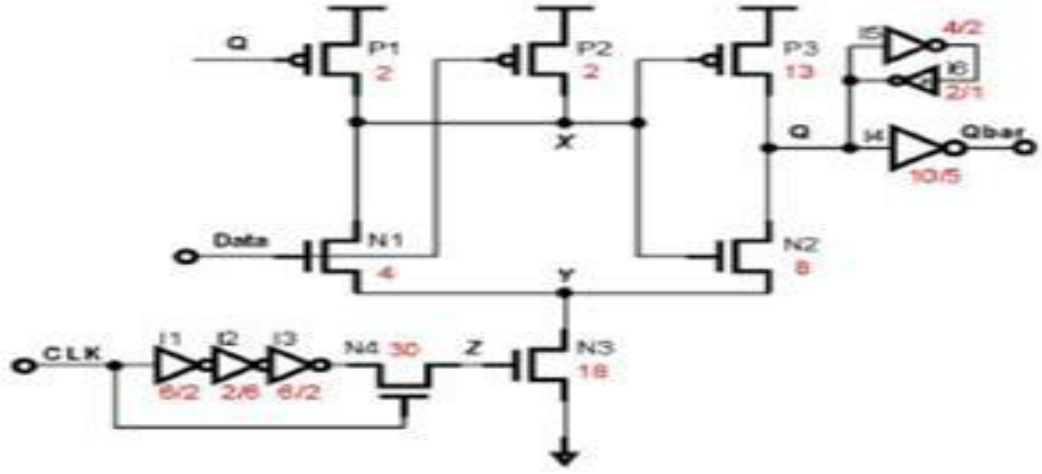

Fig. 1(b) MHLLF

3. SCCER

A refined low power P-FF design named SCCER using a conditional discharged technique. In this design, the keeper logic (back-to-back inverters I7 and I8 in Fig. 1(a) is replaced by a weak pull up transistor P1 in conjunction with an inverter I2 to reduce the load capacitance of node.

The discharge path contains n MOS transistors N2 and N1 connected in series. In order to eliminate superfluous switching at node, an extra n MOS transistor N3 is employed. Since N3 is controlled by Q_fdbk, no discharge occurs if input data remains high. The worst case timing of this design occurs when input data is "1" and node is discharged through four transistors in series, i.e., N1 through N4, while combating with the pull up transistor P1. A powerful pull-down circuitry is thus needed to ensure node can be properly discharged.

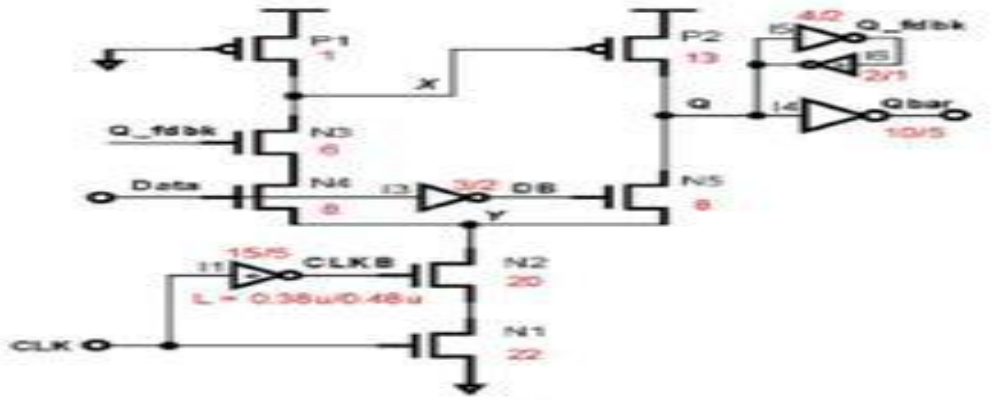

Fig. 1(c) SCCER

This implies wider N1 and N2 transistors and a longer delay from the delay inverter I1 to widen the discharge pulse width.

II. PROPOSED MODEL

The proposed model is a implicit type pulse triggered flip-flop with a conditional pulse enhancement scheme. There are two measures employed to overcome the draw backs in the conventional designs. Due to the presence of the large number of transistors in the discharge path the delay is high and also large power is consumed in power-up of the transistors. So, the number of nMOS transistors in the discharging path should be reduced. Also there is a need to increase the pull down strength when the input data=1. So there is a need to conditionally enhance the pull down strength when input data is "1." This design inherits the upper part of the SCCER design. Transistor stacking design of ip-DCO in Figure 4.4 and SCCER in Figure 4.6, is replaced by removing the transistor N2 from the discharging path. Transistor N2 and N3 are connected in parallel to form a two-input pass transistor logic (PTL)-based AND. It controls the discharge of transistor N1. The input to the AND logic is always complementary to each other. As a result, the output node is kept at zero most of the time. There is a floating node when both input signals equal to "0". But it doesn't provide any harm to the circuit performance. The critical circumstance occurs only when there is rising edges at the clock pulse. Transistors N2 and N3 are turned ON together in this case to pass a weak logic high to node. This weak pulse strength is enhanced by switching ON the transistor N1 by a time span equal to the delay provided by inverter I1. The switching power at node can be reduced due to a diminished voltage swing. Unlike the MHLLF design, where the discharge control signal is driven by a single transistor, parallel conduction of two nMOS transistors (N2 and N3) speeds up the operations of pulse generation. On designing the flip-flop in this way, the number of transistors in the discharging path can be reduced. This speeds up the pulse generation and hence delay is reduced. The area overhead is also reduced.

The flip-flop using the conditional enhancement scheme is given in the figure 1(d).

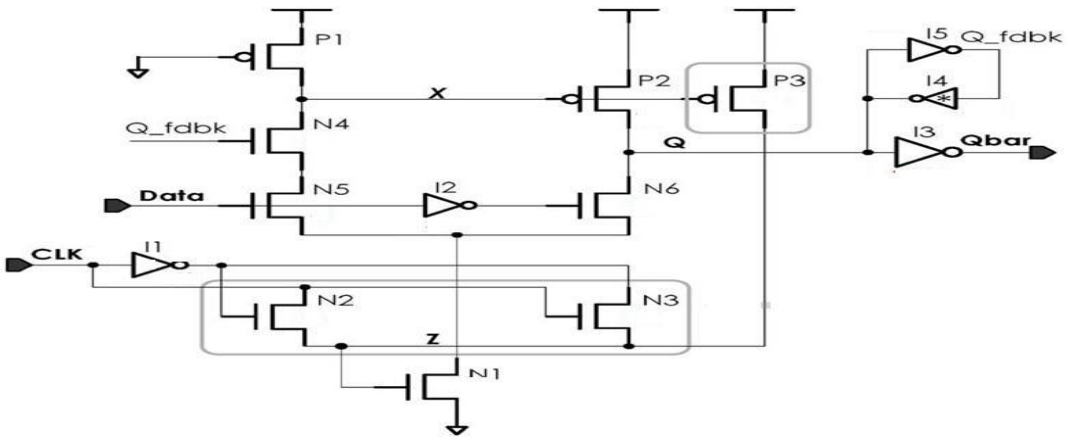

Fig. 1(d) PROPOSED

Pulses that trigger discharging are generated only when there is a need, so unwanted circuit activity due to glitches can be avoided which reduces the overall power consumption. Pulse discharge can be made faster. The delay inverters which consume more power for stretching the pulse width are replaced by the PMOS transistors which enhances the pull down strength when there is a longer discharge path. Transistor sizes are also reduced to provide area and power saving.

III. SIMULATION RESULTS

A simulation window appears with inputs and output. The power consumption is also shown on the right bottom portion of the window. If you are unable to meet the specifications of the circuit change the transistor sizes. Generate the layout again and run the simulations till you achieve your target delays. Depending on the input sequences assigned at the input the output is observed in the simulation. To demonstrate the superiority of the proposed design, post layout simulations on various P-FF designs were conducted to obtain their performance figures. These designs include the three P-FF designs shown in Fig. 1 ip-DCO MHLLF, SCCER, another P-FF design called conditional capture FF (CCFF) , and two other non-pulse triggered FF designs, i.e., a sense-amplifier-based FF (SAFF) [2], and a conventional transmission gate-based FF (TGFF). The target technology is the UMC 90-nm CMOS process. The operating condition used in simulations is 500 MHz/1.0 V. Since pulse width design is crucial to the correctness of data capturing as well as the power consumption, the pulse generator logic in all designs are first sized to function properly across process variation. All designs are further optimized subject to the tradeoff between power and D-to-Q delay, i.e., minimizing the product of the two terms.

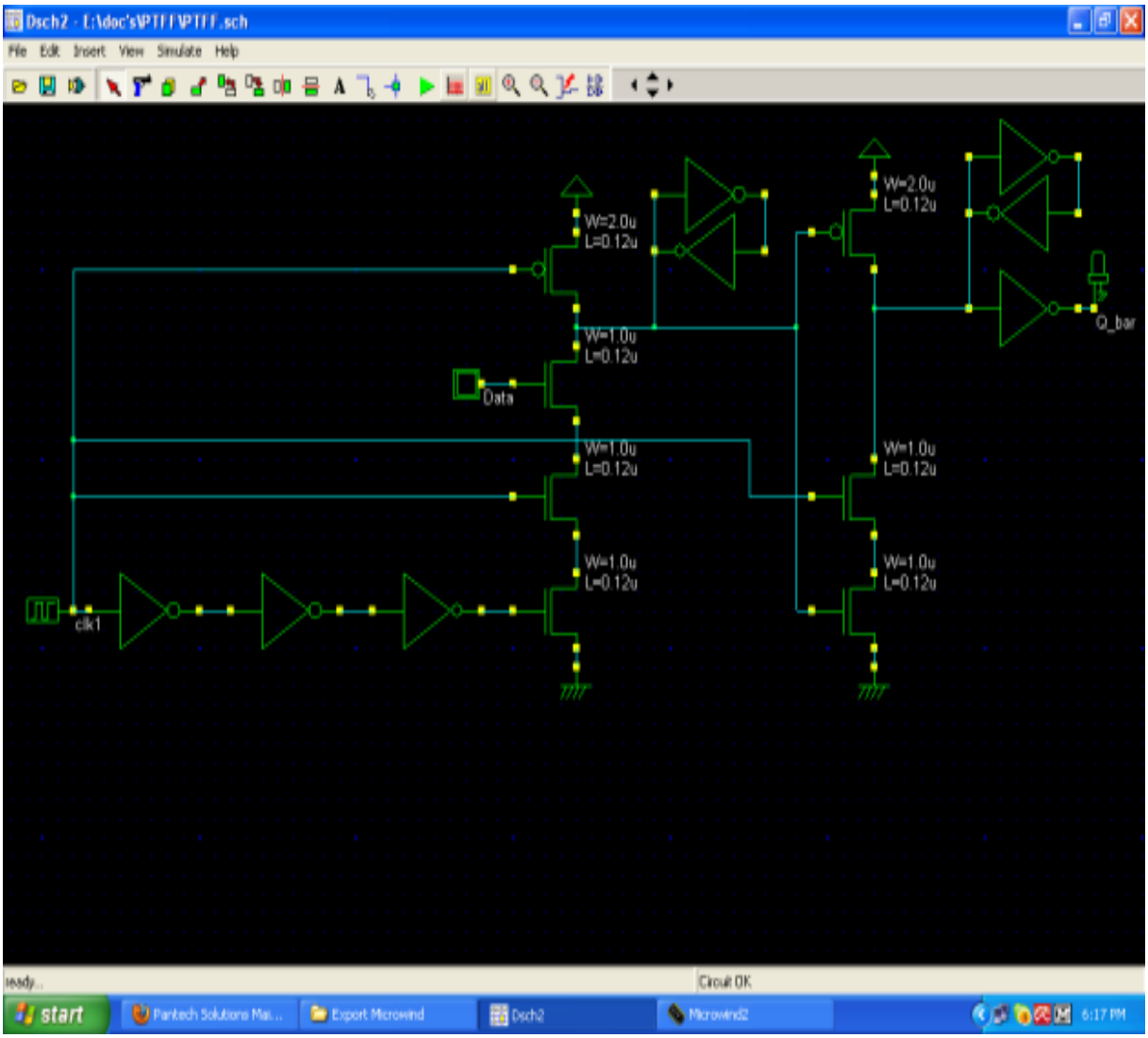

Fig. 2(a) ip-DCO in Microwind

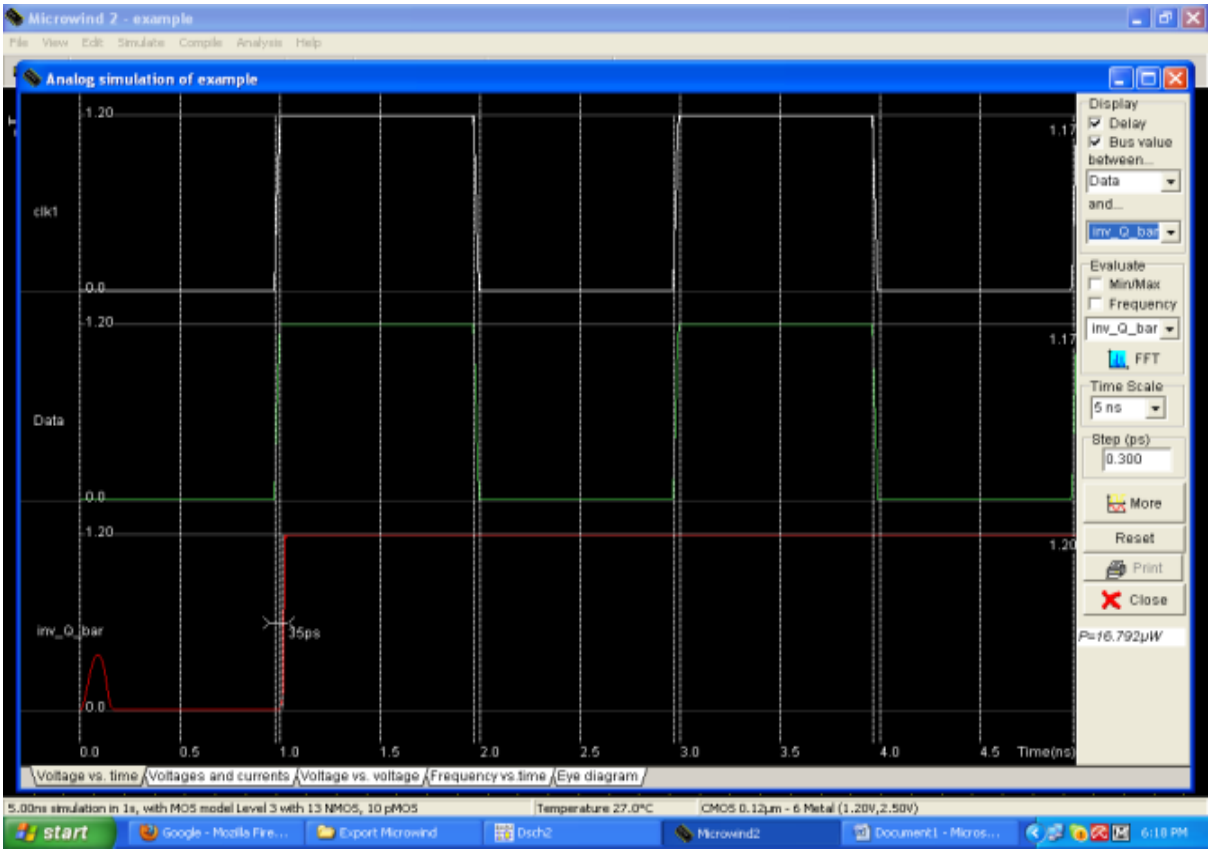

Fig. 2(b) ip-DCO waveform in Microwind

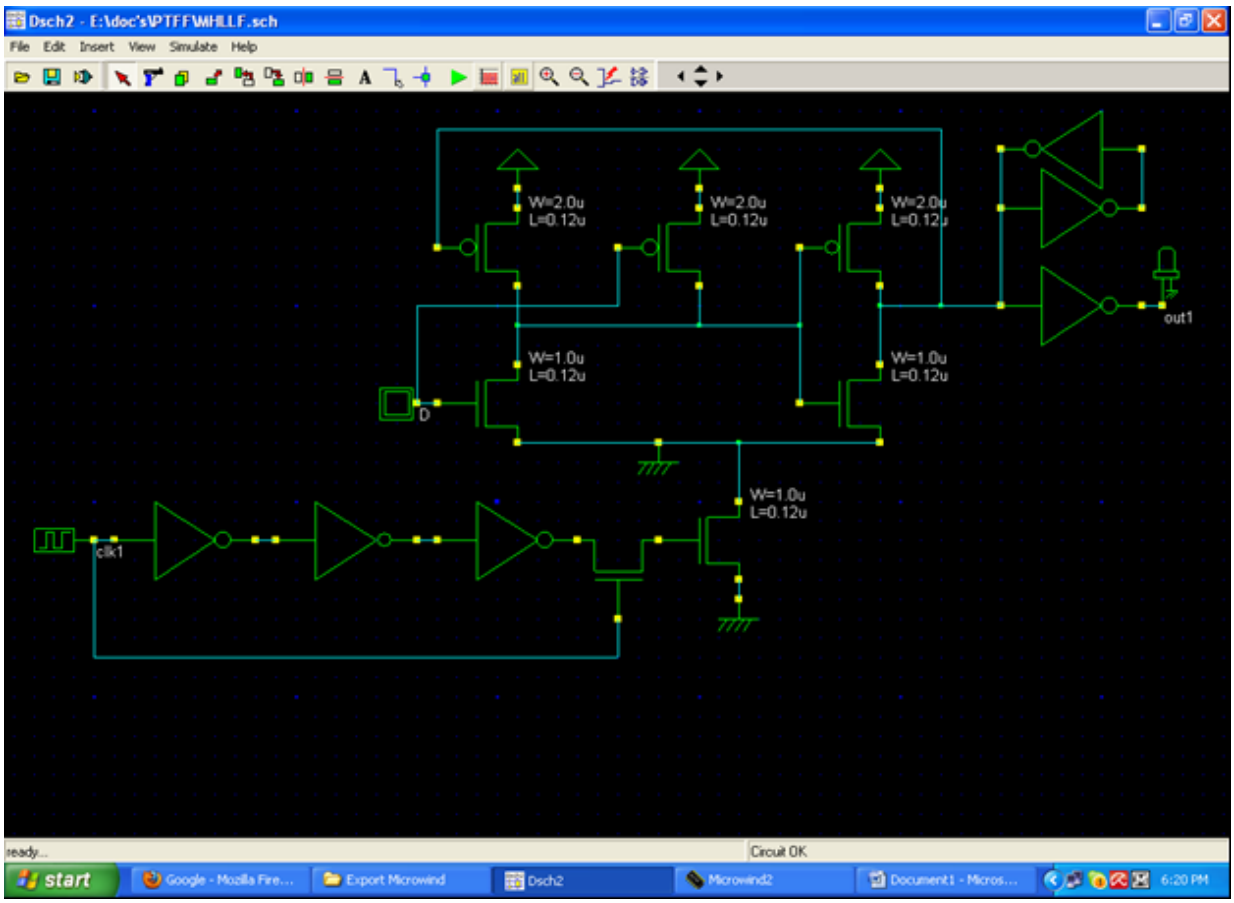

Fig. 2(c) MHLLF in Microwind

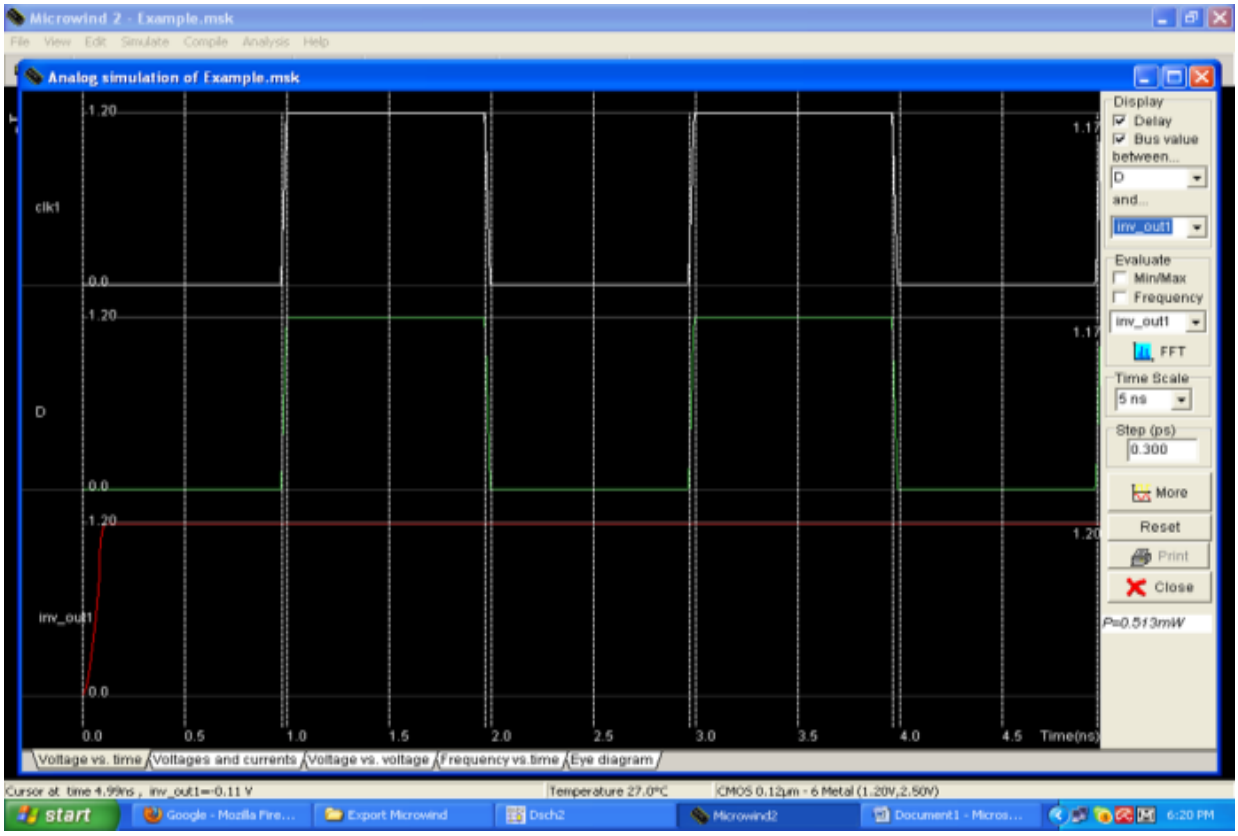

Fig. 2(d) MHLLF waveform in Microwind

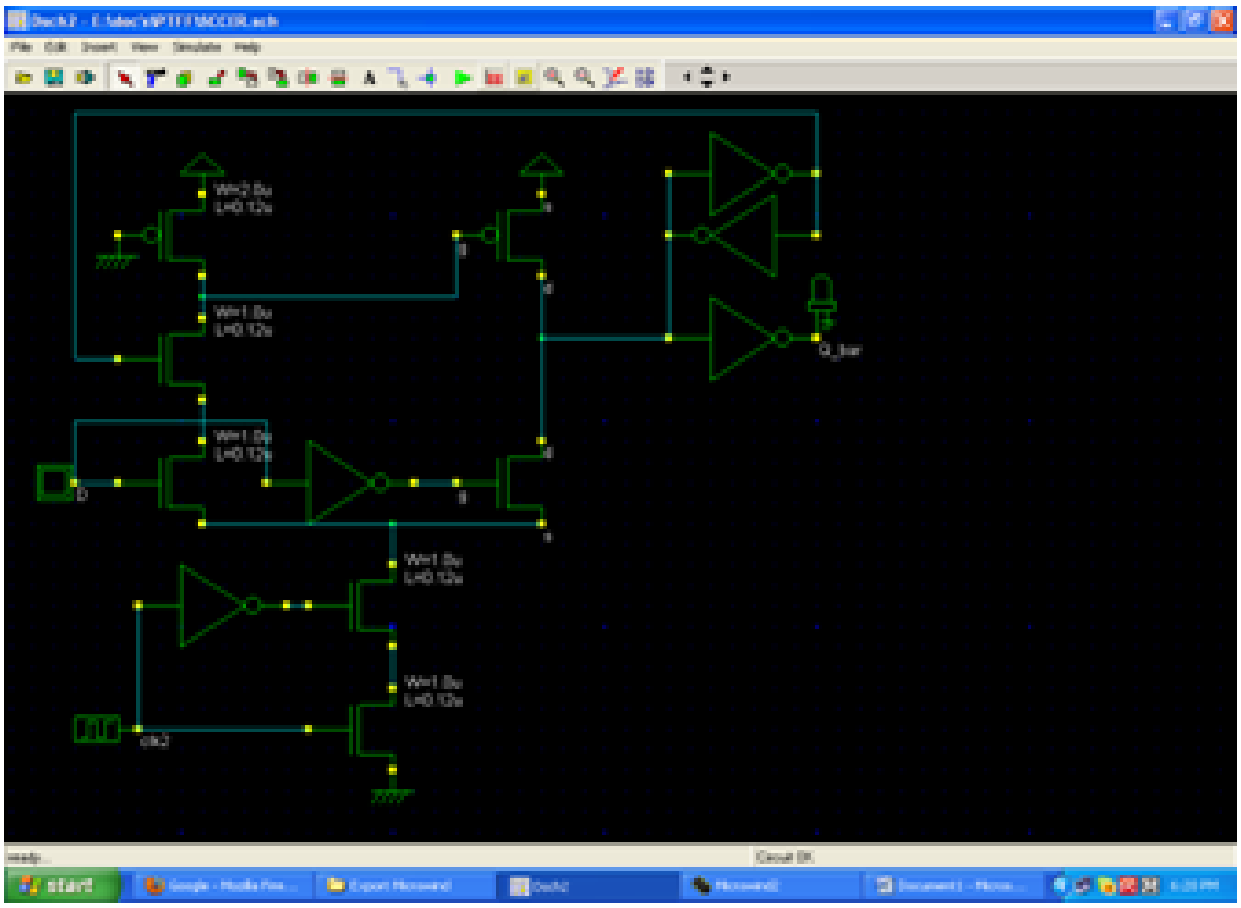

Fig. 2(e) SCCER in Microwind

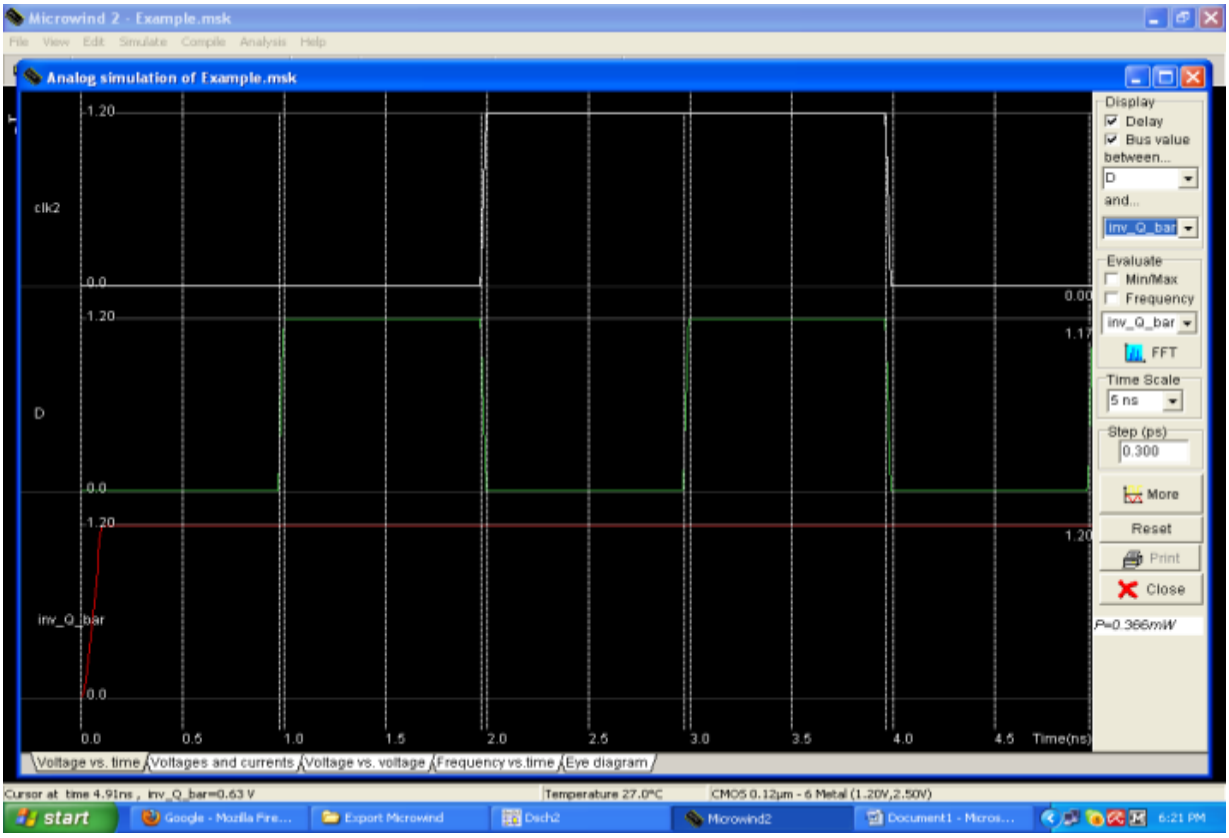

Fig. 2(f) SCCER waveform in Microwind

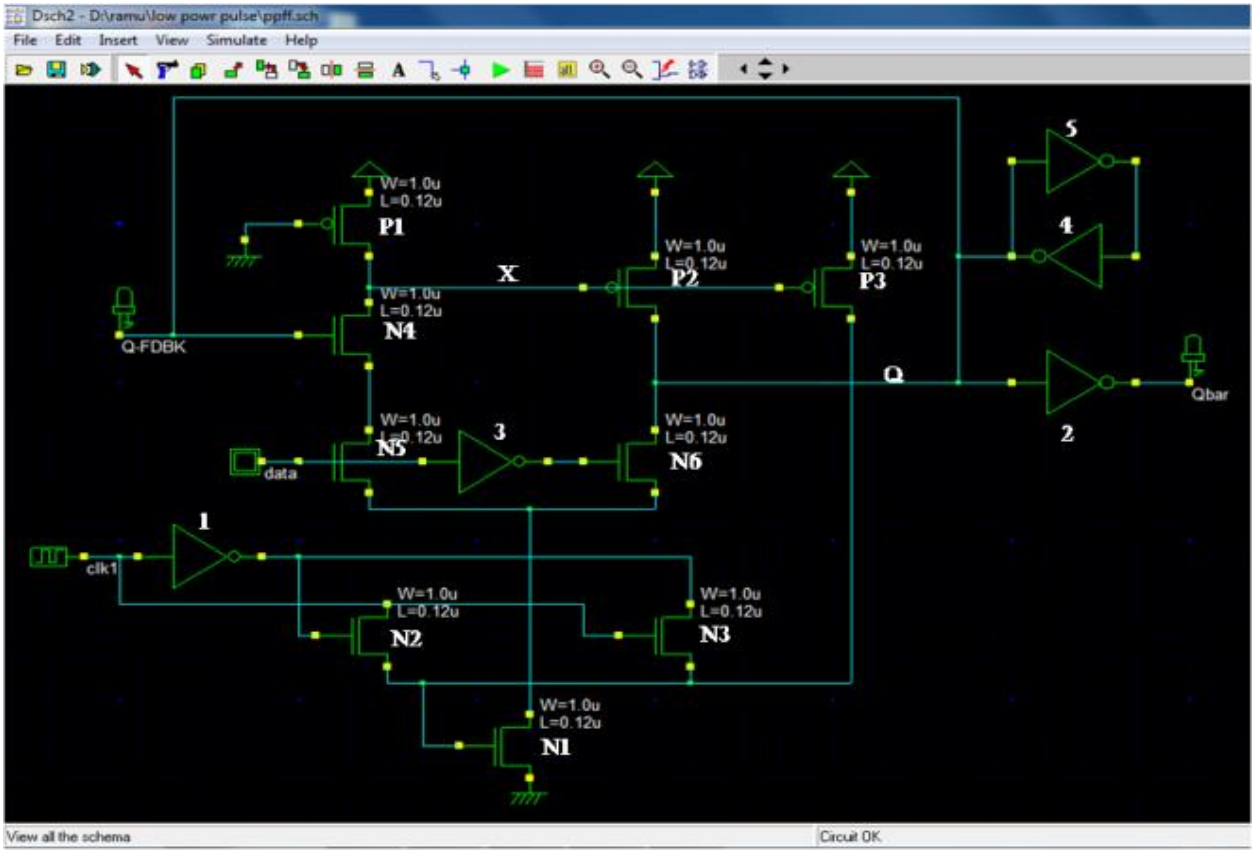

Fig .2(g) PROPOSED circuit

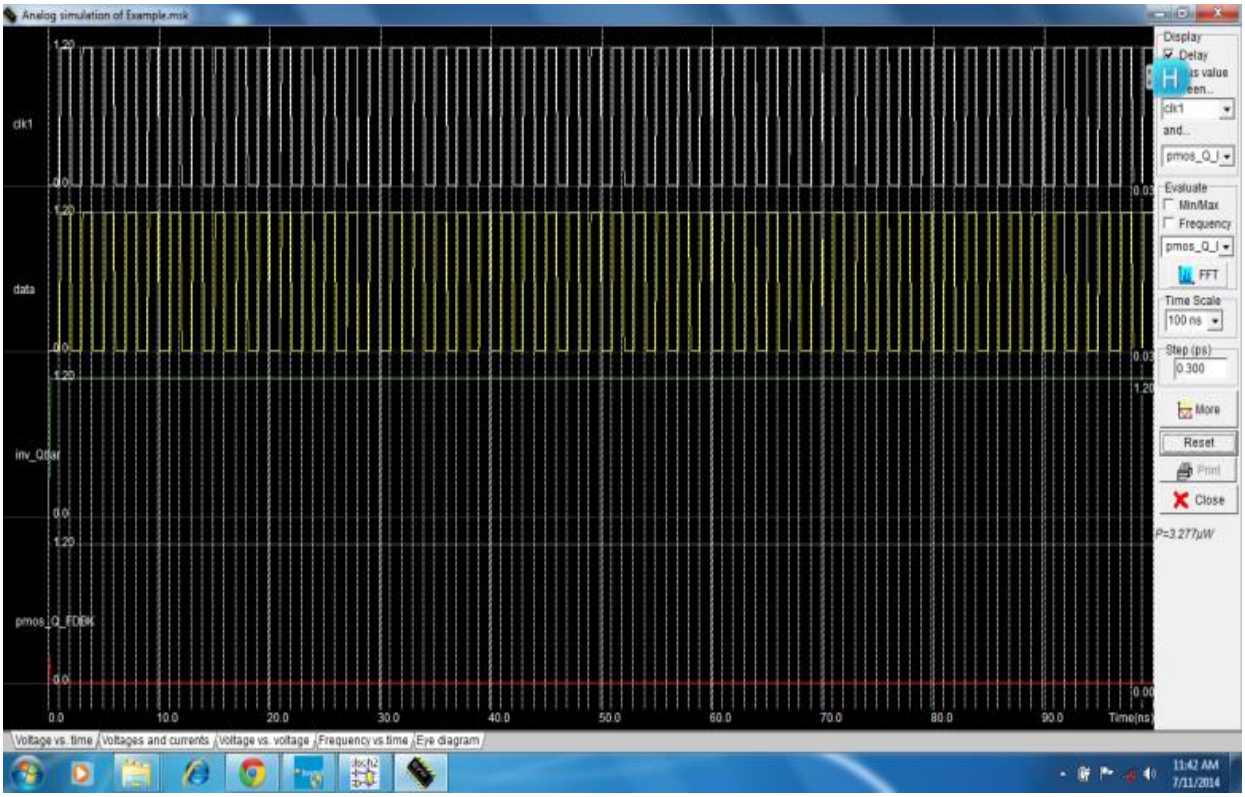

Fig. 2(h) proposed system wave forms

These are the simulation block and its results of ip-DCO, MHLLF and SCCER in Microwind.

IV. COMPARISON TABLE

Table: 1 Comparison of designed methods

P-FF	IP-DCO	MHLFF	SCCER	PROPOSED
No. of transistors/ Layout area (µm2)	23/91.88	19/93.02	17/80.07	19/79.17
Min. D-Q Delay (pS)	118.75	117.01	112.90	107.24
Avg. Power (µW)	17.50	18.97	19.40	12.90
Power Delay Product	4.22	4.89	3.19	2.65

From the designed methods the various parameters are tabulated and compared. With this comparison results the Proposed FF performed better than other two designed methods.

V. CONCLUSION

In this paper, a novel low-power pulse-triggered flip-flop (FF) design is presented. In this the clock generation circuitry an AND function is removed and is replaced with a Pass-Transistor logic based AND gate. Since in the PTL-style AND gate the n-mos transistors are in parallel they consume less power and provides a faster discharge of the pulse.A software package called the TANNER EDA tools utilizing MOSIS 90nm technology is used for the study. The comparison of the Number of transistors used and the Average power consumed for 100% activity, 50% activity and 0% activity are done. The power consumed is for five cycles of operation. The power consumption shows a decreasing trend as the switching activities are reduced. From the above results it is clear that this type of design approach can be implemented in real space systems to increase the efficiency as well as to minimize the power consumption.

Future Work

In the future Dual edge triggered flip-flop can be designed. By designing the clock generation circuit that will operate in both positive and negative level triggering (i.e., it can able to trigger in both rising and falling edge of the clock pulse). This method overcomes the single edge triggering and also reduces the power consumption.

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